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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WEINMAN, SEAN M	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,165	SONE, MASAHIRO	
	Examiner	Art Unit	
	Sean Weinman	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 28 January 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/28/04-10/26/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 are presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3 and 4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 3 recites "a preset level" on line 8. It is unclear whether this is the same as or different from the "preset level" recited in claim 1 line 26. Additionally, claim 3 recites "a current balancing circuit" on lines 13 and 20. It is unclear whether these are the same as of different from the "current balancing circuit" recited in claim 1 line 29.

5. Claim 4 recites "a current balancing circuit" on line 15. It is unclear whether this is the same as or different from the "current balancing circuit" recited in claim 1 line 29.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being anticipated by Taroda et al. (US Patent No. 5,724,542) in view of Elek et al. (US Patent Application No. 2002/0188383).

As per claim 1, Taroda et al. teach the invention, comprising:

A storage control device comprising (Figure 28):

a first I/O control unit (Figure 22 Reference 30 Group 0), including a channel control unit being connected with an information processing device (Col. 9 lines 58-65 and Col. 10 lines 15-23), a disk control unit being connected with one or more HDDs (Hard Disk Drives) (Col. 9 lines 58-65 and Col. 13 lines 10-18), a cache memory (Col. 9 lines 58-65 and Col. 10 lines 15-23 and Col. 13 lines 10-18), and a connection unit (Figure 22 [Data Bus] and Col. 10 lines 34-44);

a second I/O control unit (Figure 22 Reference 30 Group 1 and Col. 10 lines 56-65);

8. Taroda et al. do not teach two or more power supplies having a current balancing circuit for each of the I/O control units along with at least three circuit breakers for receiving electric power from a outside source. Specifically, Taroda et al. teach a storage control device with a first I/O control unit that contains a channel control unit, disk control unit, cache memory, and a connection unit along with a second I/O control unit with equal current consumption. Additionally, Taroda et al. teach where each I/O control unit has individual power supply units (Figure 22 References 39a and 39a`). However, Taroda et al. fails to detail that there are two or more power supply units having a current balancing circuit for each of the I/O control units. Additionally, Taroda et al. fails to detail that electric power is received from a outside source through at least three circuit breakers. One of ordinary skill in the art would have been motivated to look

for a teaching for a power system in which system is fed from two or more power supplies, which contain a power balancing circuit:

9. Elek et al. teach another power system which provides multiple power supply units, which contain a power balancing circuit, to power a single system.

two or more first power supply devices supplying electric power to the first I/O control unit (Figure 2 and Paragraph [0062] lines 1-4);

two or more second power supply devices supplying electric power to the second I/O control unit (Figure 2 and Paragraph [0062] lines 1-4);;

and at least three circuit breakers receiving electric power supplied from outside and supplying the electric power to the first and second power supply devices (Paragraph [0061] lines 3-6. Additionally, it is obvious to one of ordinary skill in the art that circuit breakers interrupt the supply of electricity when the current exceeds a preset level)

each of the first/second power supply devices includes a current balancing circuit (Claim 29 and Figures 3 Reference 600 and Figure 2 Reference 1000). In summary, Elek et al. teaches a power system having two or more power supplies supplying each unit having a current balancing circuit for each unit along with at least three circuit breakers for receiving electric power from a outside source.

10. It would have been obvious to one of ordinary skill in the art to combine the teachings of Taroda et al. and Elek et al. because they both teach power system which use separate power supplies to power individual system units. Elek et al. covers the deficiency of Taroda et al. by teaching the detail of two or more power supply units

having a current balancing circuit for each of the I/O control units. Additionally, that electric power is received from a outside source through at least three circuit breakers.

11. As per claim 2-5, Elek et al. teaches the power system where the power supply unit includes a AC-DC converter.

electric power supplied from outside to the circuit breakers is AC (Alternating-Current) power, and the first power supply device includes an AC-DC conversion unit for converting the AC power into DC (Direct-Current) power

the second power supply device includes an AC-DC conversion unit for converting the AC power into DC power and thereby supplies the DC power (Figure 2 and Figure 3).

12. Elek also teaches the power systems where the inputs to the power supply units are three-phase AC power. Additionally, Elek et al. teach the power system where the power supply units include a three-phase AC -DC converter.

electric power supplied from outside to the circuit breakers is three-phase AC (Alternating-Current) power (Figure 2 and Figure 3)

the first power supply device includes three AC-DC conversion units (Figure 2 and Figure 3)

the second power supply device includes three AC-DC conversion (Figure 2 and Figure 3)

13. As per claim 6, Taroda et al. and Elek et al. for the reasons discussed hereinabove teach a storage control device with a first I/O control unit that contains a channel control unit, disk control unit, cache memory, and a connection unit along with a

second I/O control unit with equal current consumption having of two or more power supply units having a current balancing circuit and a three-phase AC-DC converter for each of the I/O control units. Additionally, that three-phase electric power is received from an outside source through at least three circuit breakers.

14. As per claim 7, it is directed to the control method of the storage control device as set forth in claim 1-6. Since Taroda et al. and Elek et al. teach the claimed storage control device, Taroda et al. and Elek et al. teach the method for operating the claimed storage control device.

15. Claim 8 is rejected under 35 U.S.C. 103(a) as being anticipated by Taroda et al. (US Patent No. 5,724,542) in view of Elek et al. (US Patent Application No. 2002/0188383) as applied to claims 2-7 above, and further in view of Fisher et al. (US Patent No. 4,290,007).

16. Taroda et al. and Elek et al. teach a storage control device with a first I/O control unit that contains a channel control unit, disk control unit, cache memory, and a connection unit along with a second I/O control unit with equal current consumption having of two or more power supply units supplied by a outside source for each of the I/O control units. However, Taroda et al. and Elek et al. fail to detail the invention where the circuit breakers include a current balancing circuit for equalizing the output currents.

17. Fisher et al. teaches a power control circuit where the circuit breakers include a circuit, which balances the current flow and output of each of the breakers.

Each of the three circuit breakers includes a current balancing circuit (Col. 4 lines 40-48 and lines 51-55). In summary, Fisher et al. teaches a power control circuit which

contains circuit breakers that include current balance circuits for equalizing the current flow and output from the circuit breakers.

18. It would have been obvious to one of the ordinary skill in the art to combine the teachings of Taroda et al. and Elek et al. along with Fisher et al. because they teach a protected power system for a storage system. Fisher et al. covers the deficiency of Taroda et al. and Elek et al. by teaching the detail of the circuit breakers including a current balancing circuit to equalize the current flow and output from the circuit breakers.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean Weinman whose phone number is (571) 272-2744. The examiner can normally be reached on Monday-Friday from 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sean Weinman
Examiner
Art Unit 2115